**18ECC350T COMPREHENSION**

**Digital Electronics**

**QUESTION BANK**

1. Number Systems
2. Logic gates and Boolean Algebra, K-Map
3. Combinational Logic Circuit
4. Sequential logic circuit
5. Digital Logic Families
6. **Number System**

**Q.1** The (100110)2 is numerically equivalent to

1. (26)16 2. (36)10 3. (46)8  4. (212)4

The correct answer is/are

(A) 1, 2, and 3 (B) 2, 3, and 4 (C) 1, 2, and 4 **(D) 1, 3, and 4**

**Q.2** If (211) x = (152)8, then the value of base x is  
(A) 6 (B) 5 **(C) 7** (D) 9

**Q.3 A** computer has the following negative numbers stored in binary form as shown. The wrongly stored number is

(A) -37 as 1101 1011 (B) -89 as 1010 0111

**(C) -48 as 1110 1000** (D) -32 as 1110 0000

**Q.4** Convert the binary number 1001.00102 to decimal.

(A)90.125 **(B)9.125** (C)125 (D)12.5

**Q.5** Convert 59.7210 to BCD.

(A) 111011 **(B) 01011001.01110010** (C) 1110.11 (D) 0101100101110010

**Q.6** One Nibble contain the number of bits equal to

(A) 2 **(B) 4** (C) 8 (D) 16

1. **Logic Gates and Boolean Algebra**

**Q.7** The Boolean function a + (a̅ b) is equivalent to

(A) a.b **(B)a + b** (C) a̅.b (D) a̅ + b

**Q.8** Which of the following logical circuits is/are equivalent?

1. F1 Madhuri Engineering 30.08.2022 D1 2.F1 Madhuri Engineering 30.08.2022 D2

3. F1 Madhuri Engineering 30.08.2022 D3 4. F1 Madhuri Engineering 30.08.2022 D4

(A) 1,2 and 3 (B)2, 3 and 4 (C)1, and 2 **(D) 1,3 and 4**

**Q.9** The expression for Absorption law is given by \_\_\_\_\_\_\_\_\_

**(A) A + AB = A** (B) A + AB = B (C) AB + AA’ = A (D) A + B = B + A

**Q.10** Canonical form is a unique way of representing \_\_\_\_\_\_\_\_\_\_\_\_

(A) SOP **(B) Minterm** (C) Boolean Expressions (D) POS

**Q.11** Derive the Boolean expression for the logic circuit shown below:

Table

Description automatically generated

**(A) C(A+B) DE** (B)ABCDE (C)(A+B)(C+D)E (D)(A+B+C+D)E

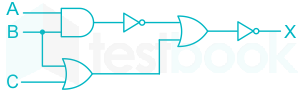
**Q.12** Which one of the following is NOT a valid identity?

(A) (x ⊕ y) ⊕ z = x ⊕ (y ⊕ z) **(B) (x + y) ⊕ z = x ⊕ (y + z)**

(C) x ⊕ y = x + y, if xy = 0 (D) x ⊕ y = (xy + x'y')'

1. **Combinational Logic Circuit**

**Q.13** For the inputs (i) A = 0, B = 1, C = 1, and (ii) A = 1, B = 1, C = 1, the respective outputs for the following circuit are



1. 0,0 (B) 1,1 (C) 0,1 (D) 1,0

**Q.14** How many FAs & HAs are required to include a 16-bit number?

(A) 8 HAs, 8 FAs **(B)1 HA, 15 FAs** (C)15 HAs, 1 FA (D)12 FAs 4 HAs

**Q.15** Number of 2 × 1 Multiplexers are required to implement 64 × 1 Multiplexers

**(A) 63** (B) 61 (C) 62 (D) 60

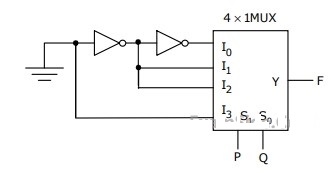
**Q.16** The network shown in fig. implements

Diagram

Description automatically generated

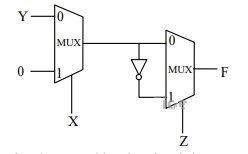
(A) AND gate **(B) NAND gate** (C)XOR gate (D) OR

Q.17 The logic function implemented by the circuit below is (ground implies a logic "0")



1. F=AND(P,Q) (B) F=OR(P,Q) (C)F=XNOR(P,Q) **(D) F= XOR(PQ)**

**Q.18** The Boolean expression F implemented by the circuit is



1. + XY + Z **(B) Y + XZ + Z** (C) Y + XY + Z

(D) + XZ + Z

1. **Sequential logic circuit**

**Q.19** The circuit shown in the figure is a

Diagram

Description automatically generated

(A)Toggle Flip Flop (B) JK Flip Flop (C) SR Latch **(D) Master-slave D Flip Flop**

**Q.20** When the output Y in the circuit below is ‘1’, it implies that data has

A picture containing diagram

Description automatically generated

**(A) changed from 0 to 1**  (B) changed from 1 to 0

(C) changed in either direction (D) no change

**Q.21** A master slave flip-flop has the characteristic that

(A) change in the input is immediately reflected in the output

(B) change in the output occurs when the state of the master is affected

**(C) change in the output occurs when the state of the slave is affected**

(D) both the master and the slave states are affected at the same time

**Q.22** A \_\_\_\_\_\_\_\_\_\_ counter can be implemented using three flipflops.

**(A)mod-6** (B)mod-9 (C)mod-11 (D)mod-13

**Q.23** If the registers have both shifts and parallel load capabilities, they are referred as \_\_\_\_\_\_\_\_\_.

**(A) universal shift registers**  (B) unidirectional shift registers

(C) sequential registers (D) bidirectional shift registers

**Q.24** The highest speed counter is

(A) Asynchronous counter

**(B) Synchronous counter**

(C) Ripple counter

(D) Ring counter

1. **Digital Logic Families**

**Q.25** The diode logic circuit of fig. is a

Diagram, schematic

Description automatically generated

**(A) AND gate**  (B) OR gate (C) NAND (D) NOR

**Q.26** The full forms of the abbreviations TTL and COMS in reference to logic families are

(A) Triple Transistor Logic and Chip Metal Oxide Semiconductor

(B) Tristate Transistor Logic and Chip Metal Oxide Semiconductor

**(C) Transistor-Transistor Logic and Complementary Metal Oxide Semiconductor**

(D) Tristate Transistor Logic and Complementary Metal Oxide Silicon

**Q.27** Commercially available ECL gates use two ground lines and one negative supply in order to

(A) reduce power consumption

(B) increase fan out

(C) reduce loading effect

**(D) eliminate the effect of power line glitches on the biasing circuit**

**Q.28** What is the standard TTL noise margin?

(A) 5.0V (B) 0.2V (C) 0.8V **(D)0.4V**

**Q.29** Among the digital IC families - ECL, TTL, and CMOS

(A) **ECL has the least propagation delay**

(B) TTL has largest fan out

(C) CMOS has the lowest noise margin

(D) TTL has the lowest power consumption

Q.30 Which of the following options comes under the non – saturated logic family in Digital Electronics?

**a) Emitter – coupled Logic**

b) High-Threshold Logic

c) Integrated – injection Logic

d) Diode – Transistor Logic

**Detailed solution**

**Ans.1.**

Text

Description automatically generated

**Ans.2.** (C) 2*x*2 + *x* +1 =64 + 5x8 + 2

**Ans.3.**

Graphical user interface, text

Description automatically generated

**Ans.4.** (1001.0010) ₂ = (1 × 2³) + (0 × 2²) + (0 × 2¹) + (1 × 2⁰) + (0 × 2⁻¹) + (0 × 2⁻²) + (1 × 2⁻³) + (0 × 2⁻⁴) = (9.125) ₁₀

**Ans.8.** , F1 Madhuri Engineering 30.08.2022 D6, F1 Madhuri Engineering 30.08.2022 D7, F1 Madhuri Engineering 30.08.2022 D8

**Ans.26.** N Full adder= N-1 Full adder + 1 half adder

**Ans.15.** A 64 × 1 multiplexer has 64 inputs so if we use 2 × 1 multiplexers 32 are needed in the first stage for 64 inputs, the output of these 32 multiplexers are connected to inputs of 16 multiplexers in the second stage. Similarly, in third stage, 8 (2 × 1) multiplexers are used, in fourth stage 4 are used and finally 2 (2 × 1) multiplexers in the fifth stage, 1 in the sixth stage. Total 2 × 1 multiplexers needed are 32 + 16 + 8 + 4 + 2 + 1 = 63

**Ans.16.** f1 = .0+CB=CB

f= +f1.= +CB = + = ++ =

**Ans.20.** Presently, Y = 1. This implies that prior to clock pulse; both the D-inputs were in logic ‘1’ state. This further implies that Q-output of the first flip–flop was in logic ‘0’ state. This can result from its D-input being previously in logic ‘0’ state. Hence, the data input has changed from 0 to 1.

**Ans.21.** The master flip-flop is triggered by the external clock pulse train while the slave is activated at its inversion i.e. if the master is positive edge-triggered, then the slave is negative-edge triggered and vice-versa. There will be a change in the output when the state of the slave is affected because the output is taken at the slave.

**Ans.22.** To construct a counter with any MOD number, the minimum number flip flops required must satisfy: Modulus ≤ 2n Where n is the number of flip-flops and is the minimum value satisfying the above condition.

**Ans.24.** The synchronous counter is the fastest counter because all the flip flop gets clock at the same time whereas in asynchronous counter clock is given only to input flip flop and it takes some time to reach all the flip flop.